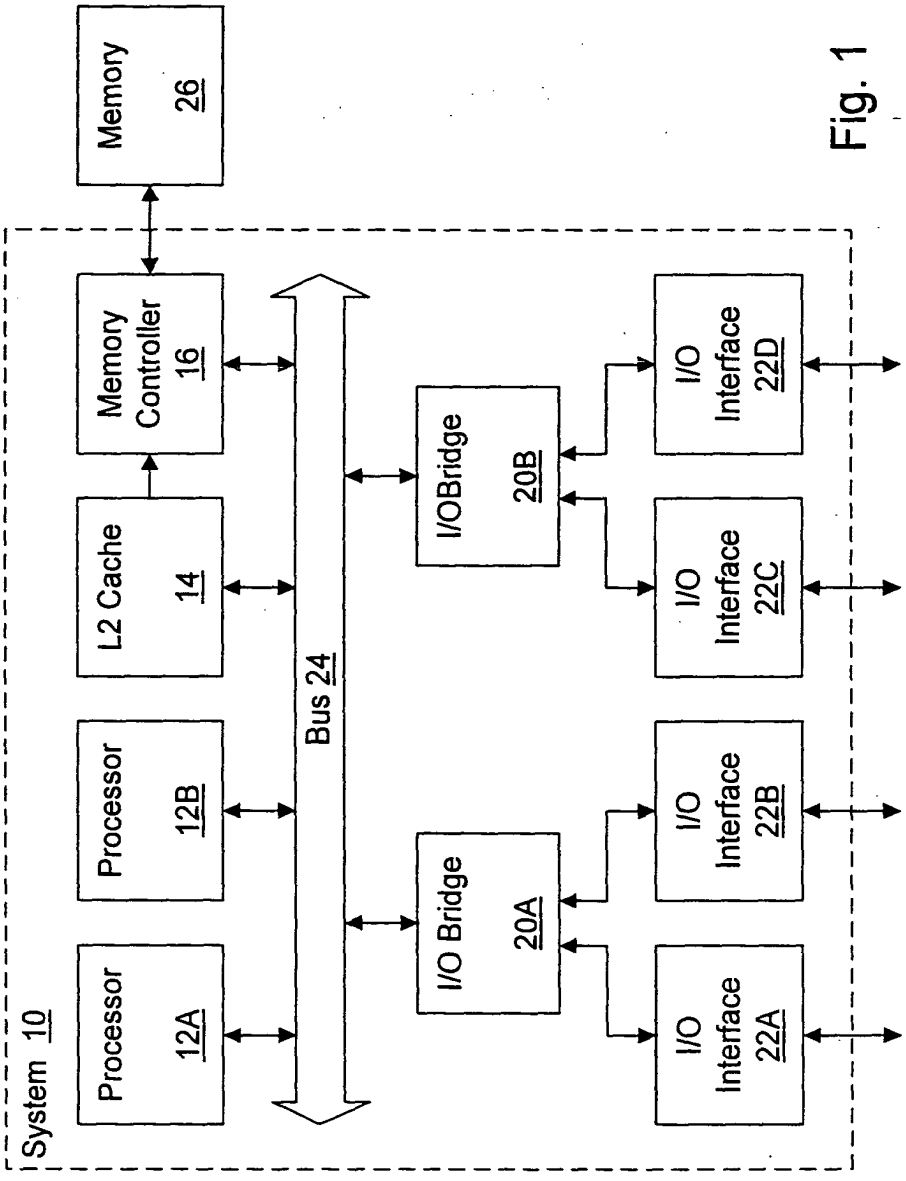
System 10
Memory 26
Memory Controller 16
L2 Cache 14
Processor 12A
Processor 12B
Bus 24
I/O Bridge 20A
I/OBridge 20B
I/O Interface 22A
I/O Interface 22B
I/O Interface 22C
I/O Interface 22D

Fig. 1

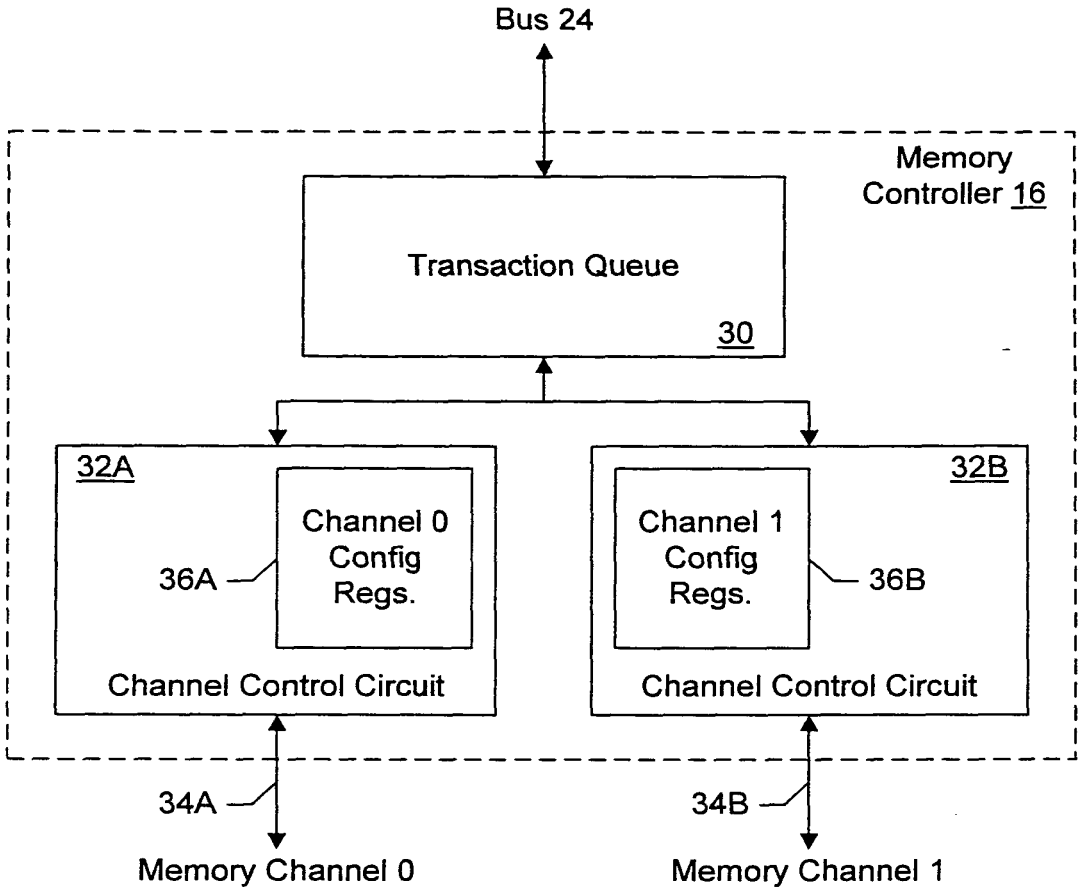
Bus 24
Memory Controller 16
Transaction Queue
30
32A
32B
Channel 0 Config Regs.
36A
Channel 1 Config Regs.
36B
Channel Control Circuit
Channel Control Circuit
34A
34B
Memory Channel 0
Memory Channel 1

Fig. 2

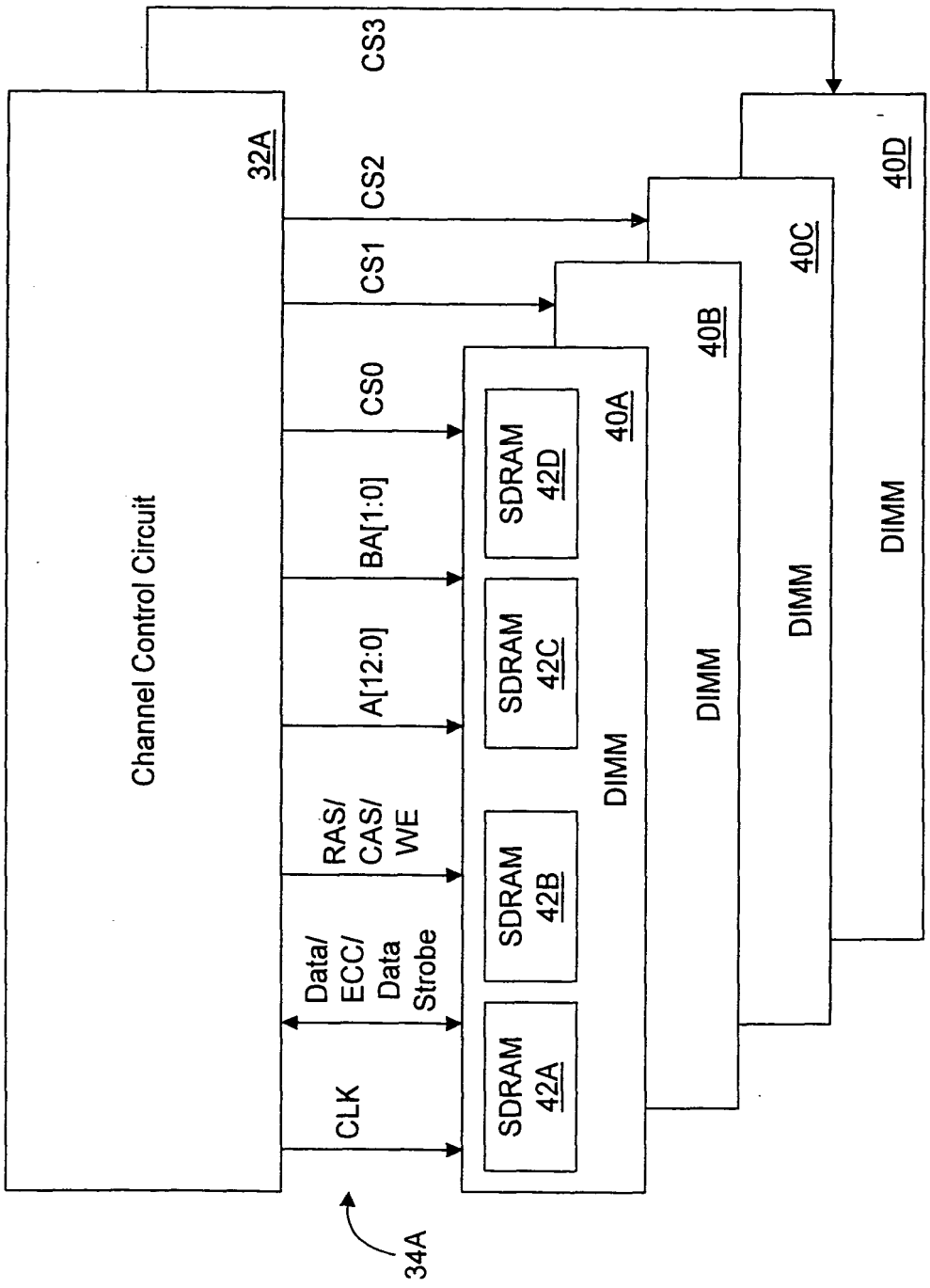
Channel Control Circuit
32A
CS3
CS2
CS1
CS0
BA[1:0]
A[12:0]
RAS/
CAS/
WE
Data/
ECC/
Data
Strobe
CLK
SDRAM
42A
SDRAM
42B
SDRAM
42C
SDRAM
42D
DIMM
40A
DIMM
40B
DIMM
40C
DIMM
40D
34A

Fig. 3

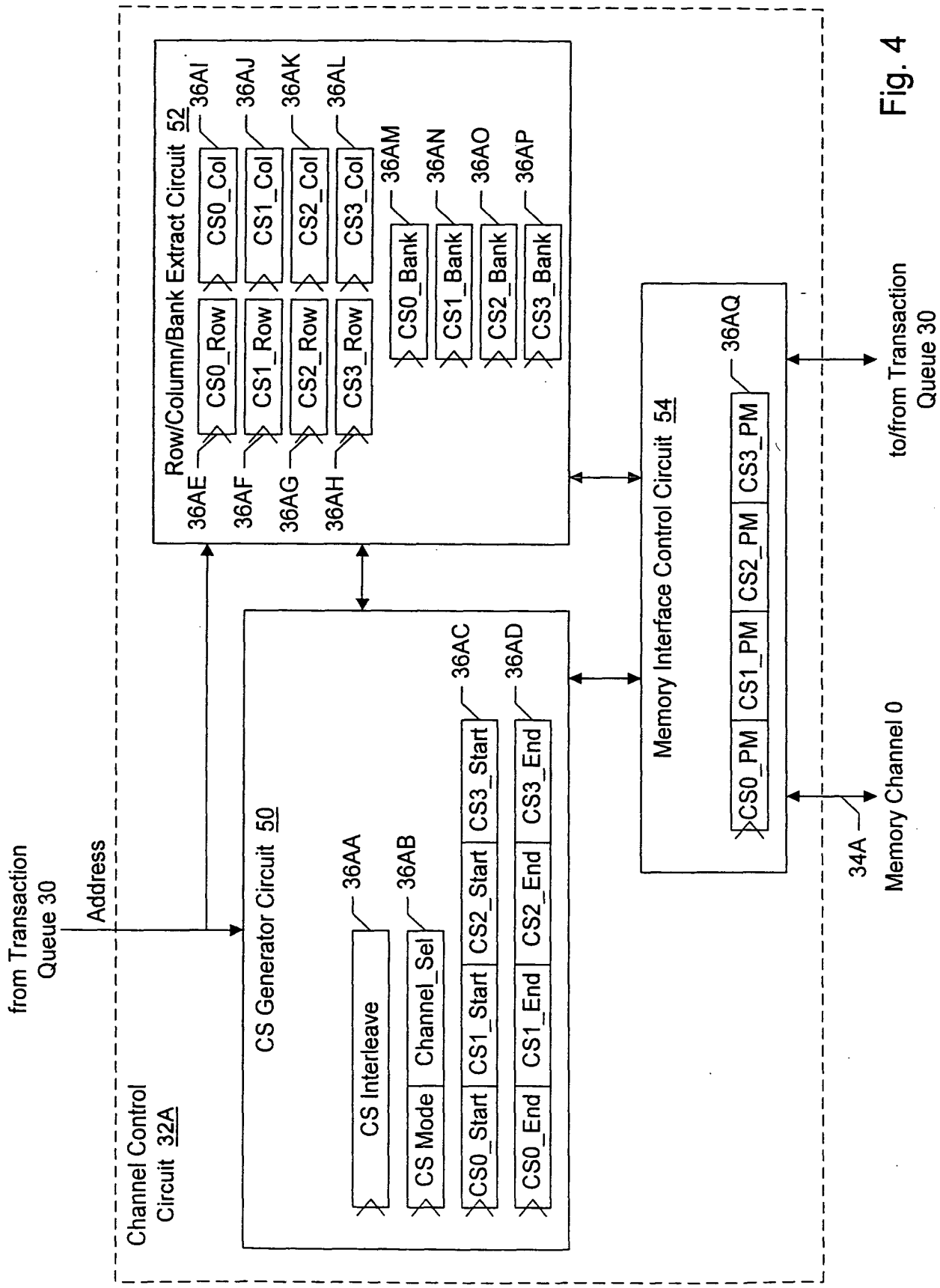
Channel Control Circuit 32A
from Transaction Queue 30
Address
CS Generator Circuit 50
CS Interleave
CS Mode
Channel_Sel
CS0_Start
CS1_Start
CS2_Start
CS3_Start
CS0_End
CS1_End
CS2_End
CS3_End
36AA
36AB
36AC
36AD
Row/Column/Bank Extract Circuit 52
CS0_Row
CS1_Row
CS2_Row
CS3_Row
CS0_Col
CS1_Col
CS2_Col
CS3_Col
CS0_Bank
CS1_Bank
CS2_Bank
CS3_Bank
36AE
36AF
36AG
36AH
36AI
36AJ
36AK
36AL
36AM
36AN
36AO
36AP
Memory Interface Control Circuit 54
CS0_PM
CS1_PM
CS2_PM
CS3_PM
36AQ
34A
Memory Channel 0
to/from Transaction Queue 30

Fig. 4

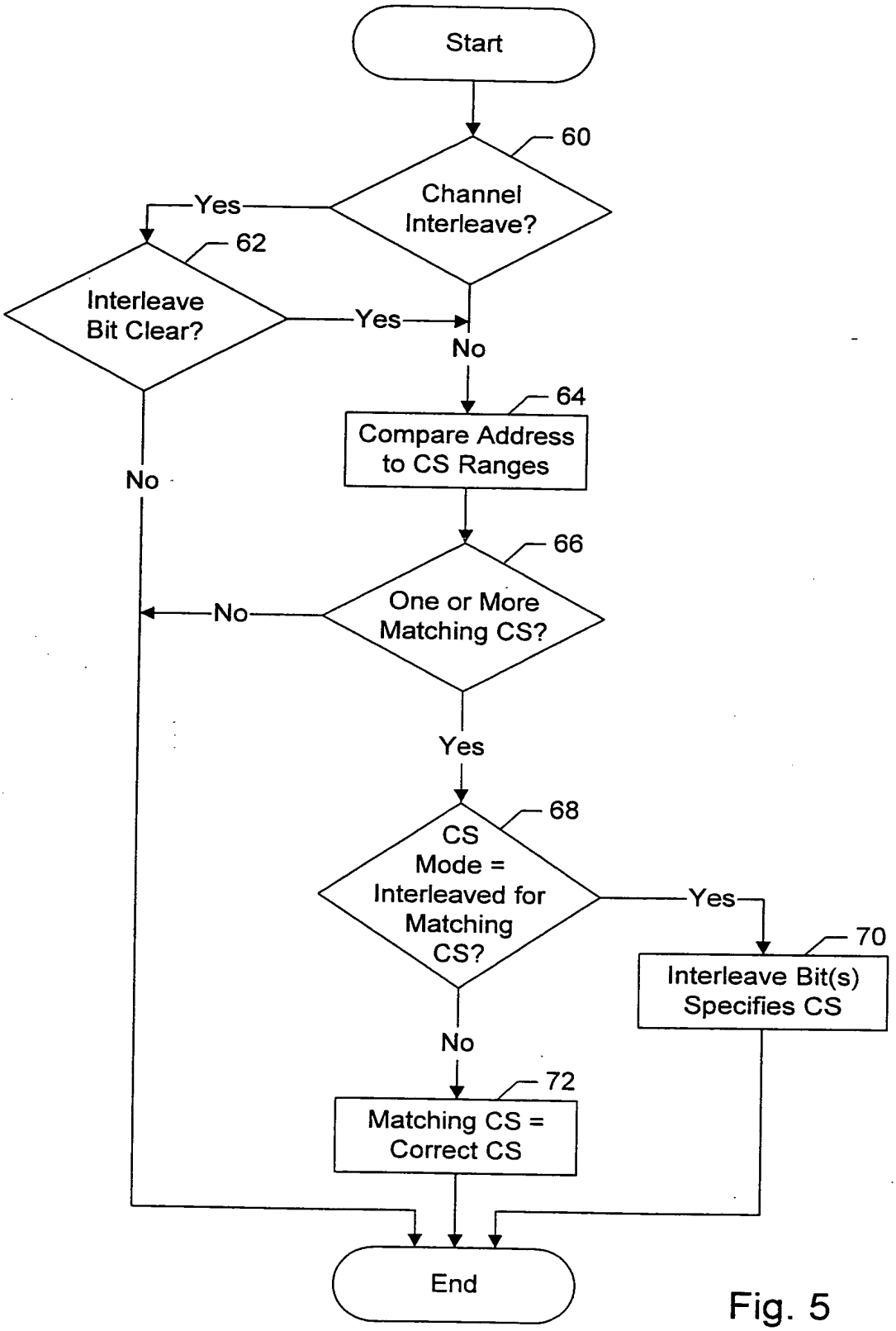
Start
60
Channel Interleave?
Yes
62
Interleave Bit Clear?
Yes
No
64
Compare Address to CS Ranges
No
66
One or More Matching CS?
No
Yes
68
CS Mode = Interleaved for Matching CS?
Yes
70
Interleave Bit(s) Specifies CS
No
72
Matching CS = Correct CS
End

Fig. 5

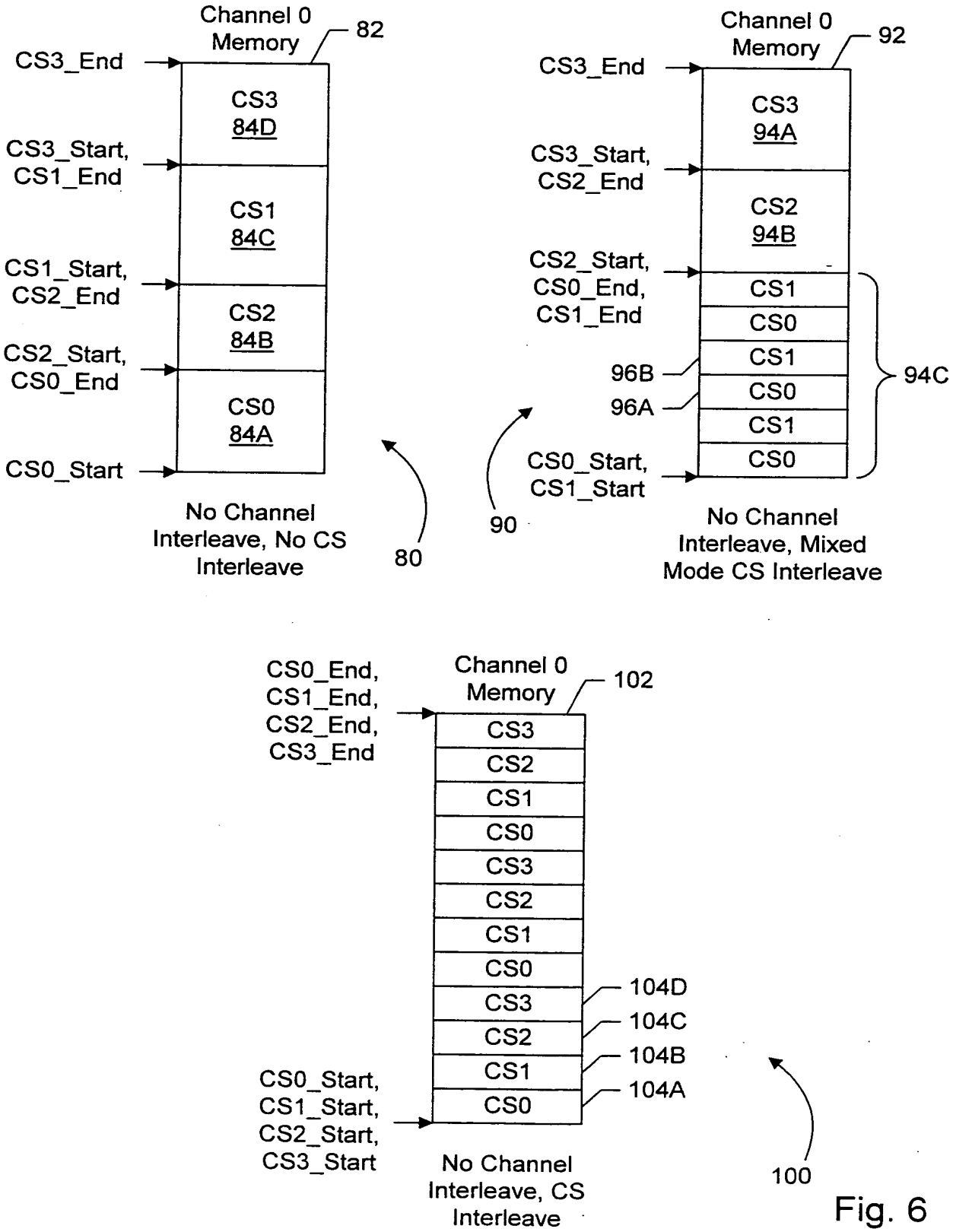
Channel 0 Memory
82
CS3_End
CS3 84D
CS3_Start, CS1_End
CS1 84C
CS1_Start, CS2_End
CS2 84B
CS2_Start, CS0_End
CS0 84A
CS0_Start
No Channel Interleave, No CS Interleave
80
Channel 0 Memory
92
CS3_End
CS3 94A
CS3_Start, CS2_End
CS2 94B
CS2_Start, CS0_End, CS1_End
CS1
CS0
CS1
CS0
CS1
CS0
96B
96A
94C
CS0_Start, CS1_Start
90
No Channel Interleave, Mixed Mode CS Interleave
CS0_End, CS1_End, CS2_End, CS3_End
Channel 0 Memory
102
CS3
CS2
CS1
CS0
CS3
CS2
CS1
CS0
CS3
CS2
CS1
CS0
104D
104C
104B
104A
CS0_Start, CS1_Start, CS2_Start, CS3_Start
No Channel Interleave, CS Interleave
100

Fig. 6

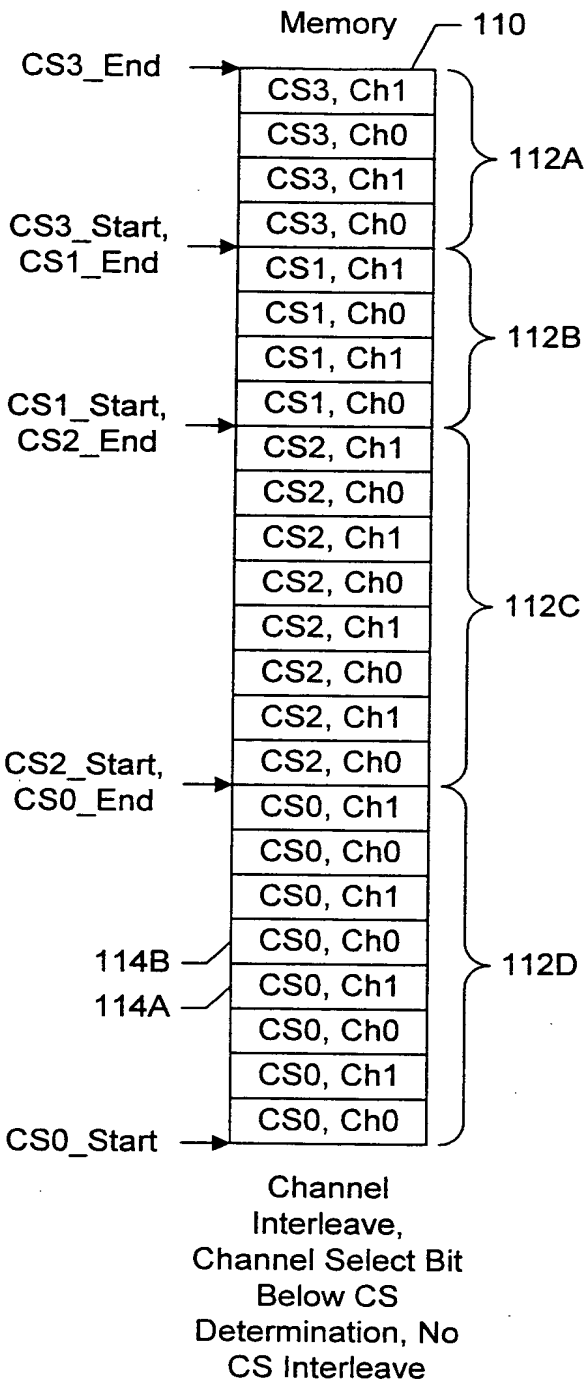
Memory
110
CS3_End
CS3, Ch1
CS3, Ch0
CS3, Ch1
CS3, Ch0
112A
CS3_Start,
CS1_End
CS1, Ch1
CS1, Ch0
CS1, Ch1
CS1, Ch0
112B
CS1_Start,
CS2_End
CS2, Ch1
CS2, Ch0
CS2, Ch1
CS2, Ch0
CS2, Ch1
CS2, Ch0
CS2, Ch1
112C
CS2_Start,
CS0_End
CS2, Ch0
CS0, Ch1
CS0, Ch0
CS0, Ch1
114B
CS0, Ch0
112D
114A
CS0, Ch1
CS0, Ch0
CS0, Ch1
CS0_Start
CS0, Ch0
Channel
Interleave,
Channel Select Bit
Below CS
Determination, No
CS Interleave

Fig. 7

512 MB CS0 Region, 4K Rows, 1K Columns

CS0_Row 36AE	00000000_00011111_11111110_00000000_00000000
CS0_Col 36AI	00000000_00000000_00000001_11111111_10000000
CS0_Bank 36AM	00000000_00000000_00000000_00000000_01100000

120

512 MB CS0 Region, 4K Rows, 1K Columns, Alternative Encoding

CS0_Row 36AE	00000000_00011111_11111110_00000000_00000000
CS0_Col 36AI	00000000_00000000_00000000_01111111_11100000
CS0_Bank 36AM	00000000_00000000_00000001_10000000_00000000

122

512 MB CS0 Region, 4K Rows, 1K Columns, 64 Byte Bank Interleave

CS0_Row 36AE	00000000_00011111_11111110_00000000_00000000
CS0_Col 36AI	00000000_00000000_00000001_11111111_00100000
CS0_Bank 36AM	00000000_00000000_00000000_00000000_11000000

124

1024 MB CS0 and CS1 Region, 4K Rows, 1K Columns

CS_Interleave 36AA	00000000_00000000_00000010_00000000_00000000
CS0_Row 36AE	00000000_00111111_11111100_00000000_00000000
CS0_Col 36AI	00000000_00000000_00000001_11111111_10000000
CS0_Bank 36AM	00000000_00000000_00000000_00000000_01100000
CS1_Row 36AF	00000000_00111111_11111100_00000000_00000000
CS1_Col 36AJ	00000000_00000000_00000001_11111111_10000000
CS1_Bank 36AN	00000000_00000000_00000000_00000000_01100000

126

Fig. 8

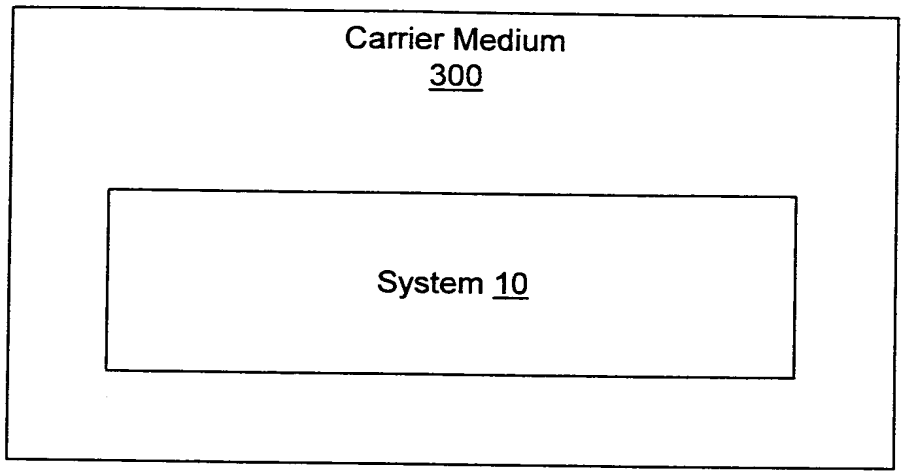

Fig. 9